IN THE DRAWINGS:

Submitted herewith is a replacement sheet for Fig. 2 incorporating a revision to overcome the drawing objection. More specifically, Fig. 2 has been revised to insert the legend "Prior Art."

REMARKS

In the last Office Action, the Examiner withdrew claims 2-7 from further consideration as being directed to a non-elected invention. The drawings were objected to because Fig. 2 is not designated with the legend "Prior Art". Claim 1 was rejected under 35 U.S.C. §102(a) as being anticipated by U.S. Patent No. 6,639,275 to Ninomiya.

In accordance with the present response, the specification has been suitably revised to correct informalities and bring it into better conformance with U.S. practice. The title of the invention has been revised to correct the spelling of "VERTICAL". A new abstract which more clearly reflects the invention to which the amended and new claims are directed has been substituted for the original abstract. A replacement sheet for Fig. 2 has been submitted incorporating a revision to overcome the drawings objection. More specifically, Fig. 2 has been revised to insert the legend "Prior Art."

Original independent claim 1 has been amended to conform the order of the steps in the method of manufacturing a vertical MOS transistor to the written description. Claim 1 has been further amended in formal respects to improve the wording and bring it into better conformance with U.S. practice. Non-elected claims 2-7 have been replaced by new

claims 8-13. New claims 8-9 and 10-13 are directed to the species of Figs. 12 and 13, respectively. Applicant respectfully submits that amended independent claim 1 is generic to all species identified by the Examiner in the August 31, 2005 Office Action. Non-elected claims 8-13 have been retained in the application pending possible withdrawal of the restriction requirement or allowance of a generic (e.g., amended independent claim 1) or sub-generic claim.

Applicant requests reconsideration of his application in light of the foregoing amendments and the following discussion.

Brief Summary of Invention

The present invention is directed to a method of manufacturing a vertical MOS transistor.

As described in the specification (pages 1-5), conventional methods of manufacturing a vertical MOS transistor have been inefficient due to the fabrication of a vertical MOS transistor which has been difficult to miniaturize and which has a poor yield and poor driving capability. For example, in the conventional vertical MOS transistor shown in Fig. 2, a contact hole 13 is formed so as to extend over a heavily doped source region 7 and a body contact region 8 during formation of the contact hole 13. As

a result, it is necessary to provide a large area for the contact hole 13 in consideration of a layout margin for deviation and alignment between both of the regions 7 and 8. In addition, in order to avoid electrical conduction between the gate electrode 6 and the source electrode 15, a space defined between the contact hole 13 and a pattern of a trench 4 needs to be set at intervals. These settings obstruct miniaturization of the vertical MOS transistor and enhancement of the yield and driving capability thereof.

The present invention overcomes the drawbacks of the conventional art. Figs. 1 and 3-11 show an embodiment of a method of manufacturing a vertical MOS transistor according to the present invention embodied in the claims. In one embodiment of the manufacturing method, an impurity of a second conductivity type is implanted into a main surface of a semiconductor substrate 1 of a first conductivity type and the impurity is thermally diffused to form a body region 3 of the second conductivity type. Anisotropic etching is then carried out on a region of the main surface of a semiconductor substrate 1 to form a trench 4. A gate oxide film 5 is formed over the main surface of the semiconductor substrate 1 and along wall surfaces of the trench 1. A polycrystalline silicon layer is deposited into the trench 4 and over the main surface of the semiconductor substrate 1 so as to overlie the

gate oxide film 5. The polycrystalline silicon layer is then etched so as to remove the polycrystalline silicon layer overlying the main surface of the semiconductor substrate 1 and so as to remove the polycrystalline silicon layer within the trench 4 to a predetermined depth from the main surface of the semiconductor substrate 1 to form a gate electrode 6 within the trench 4.

Thereafter, an impurity of the first conductivity type is implanted into the main surface of the semiconductor substrate 1 to form a source region 7 of the first conductivity type. An impurity of the second conductivity type is implanted into the main surface of the semiconductor substrate 1 to form a body contact region 8 of the second conductivity type. An intermediate insulating film 9 is deposited over the main surface of the semiconductor substrate 1 and the gate electrode 6. The intermediate insulating film 9 overlying the main surface of the semiconductor substrate is then etched back so as to entirely expose the source region 7 and the body contact region 8 forming the main surface of the semiconductor substrate 1. A source metal electrode 15 is then over the main surface of the semiconductor substrate 1. By etching back the intermediate insulating film as set forth above, formation of the source metal electrode is facilitated.

According to another aspect of the present invention, the etching back step includes the step of etching back the intermediate insulating film 9 to planarize the main surface of the semiconductor substrate 1, and the step of forming the source metal electrode 15 comprises the step of forming the source metal electrode 15 as a planar structure. By this method, the source metal electrode 15 can be formed so as to cover the entire main surface of the semiconductor substrate 1 so that a contact area between the source metal electrode and the source and body contact regions 7, 8 is increased to thereby substantially reduce a resistance therebetween.

Thus, the present invention provides a method of manufacturing a vertical MOS transistor which has an enhanced driving capability and which is well adapted for miniaturization.

Traversal of Prior Art Rejection

Claim 1 was rejected under 35 U.S.C. §102(a) as being anticipated by Ninomiya. Applicant respectfully traverses this rejection and submits that amended claim 1 recites subject matter which is not identically disclosed or described in Ninomiya.

Amended independent claim 1 is directed to a method of manufacturing a vertical MOS transistor and requires the steps of implanting an impurity of a second conductivity type into a main surface of a semiconductor substrate of a first conductivity type and thermally diffusing the impurity to form a body region of the second conductivity type, carrying out anisotropic etching on a region of the main surface of a semiconductor substrate to form a trench having a plurality of wall surfaces, forming a gate oxide film over the main surface of the semiconductor substrate and along the wall surfaces of the trench, depositing a polycrystalline silicon layer into the trench and over the main surface of the semiconductor substrate so as to overlie the gate oxide film, etching the polycrystalline silicon layer so as to remove the polycrystalline silicon layer overlying the main surface of the semiconductor substrate and so as to remove the polycrystalline silicon layer within the trench to a predetermined depth from the main surface of the semiconductor substrate to form a gate electrode within the trench, implanting an impurity of the first conductivity type into the main surface of the semiconductor substrate to form a source region of the first conductivity type, implanting an impurity of the second conductivity type into the main surface of the semiconductor substrate to form a body contact region of the

second conductivity type, depositing an intermediate insulating film over the main surface of the semiconductor substrate and the gate electrode, etching back the intermediate insulating film overlying the main surface of the semiconductor substrate so as to entirely expose the source region and the body contact region forming the main surface of the semiconductor substrate, and forming a source metal electrode over the main surface of the semiconductor substrate. No corresponding combination of steps is disclosed or described by Ninomiya.

Nimomiya discloses a method of manufacturing a vertical MOS transistor in which various steps are performed, including the formation of a gate oxide film, polycrystalline silicon layer, trench, gate electrode, body region, source region, and body contact region. However, Ninomiya does not disclose or suggest the step of depositing an intermediate insulating film and subsequent step of etching back the intermediate insulating film recited in independent claim 1. In this regard, contrary to the Examiner's contention, the element denoted by reference numeral "20" in Fig. 6A of Ninomiya corresponds to a contact hole, not to an intermediate insulating film (col. 9, line 15). In Ninomiya, the formation of the vertical MOS transistor requires the formation of a contact hole 20 which is disposed just over the source region

17 and the base region 16a, as shown in Fig. 6B (col. 9, lines 16-18). No such contact hole is required on the source region and body contact region of the vertical MOS transistor recited in independent claim 1.

In the absence of the foregoing disclosure recited in independent claim 1, anticipation cannot be found. See, e.g., W.L. Gore & Associates v. Garlock, Inc., 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984) ("Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration"); Continental Can Co. USA v. Monsanto Co., 20 USPQ2d 1746, 1748 (Fed. Cir. 1991) ("When more than one reference is required to establish unpatentability of the claimed invention anticipation under § 102 can not be found"); Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984) (emphasis added) ("Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim").

Stated otherwise, there must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention. This standard is clearly not satisfied by Ninomiya for the reasons stated above. Furthermore, Ninomiya does not

suggest the claimed subject matter and, therefore, would not have motivated one skilled in the art to modify Ninomiya's method to arrive at the claimed invention.

In view of the foregoing, applicants respectfully request that the rejection of claim 1 under 35 U.S.C. §102(a) as being anticipated by Ninomiya be withdrawn.

Applicants respectfully submit that the prior art of record also does not disclose or suggest the subject matter recited in newly added claims 8-18.

New claims 8-18 depend on and contain all of the limitations of amended independent claim 1 and, therefore, distinguish from the prior art of record at least in the same manner as claim 1.

Moreover, there are separate grounds for patentability of new claim 8-18.

Claims 8-9 are directed to the species of Fig. 12. Claim 8 includes the additional limitation that the intermediate insulating film comprises a first insulating film, and, between the implanting step to form the body contact region and the step of depositing the first insulating film, the additional steps of depositing a second insulating film over the main surface of the semiconductor substrate, and removing the first insulating film overlying the main surface of the semiconductor substrate by anisotropic etching to form

side spacers made of the second insulating film on the wall surfaces of the trench so as to overly the gate electrode. Claim 9 includes the additional limitation that the second insulating film comprises a silicon nitride film. No corresponding steps are disclosed or suggested by the prior art of record.

Claims 10-13 are directed to the species of Fig. 13. Claim 10 includes the additional limitation that the intermediate insulating film comprises a first insulating film, and, between the implanting step to form the body contact region and the step of depositing the first insulating film, the additional steps of depositing a second insulating film in a thickness so as to completely fill the trench and so as to overly and flatten the main surface of the semiconductor substrate, and etching back the second insulating film so as to remove the second insulating film overlying the main surface of the semiconductor substrate and so as to leave the second insulating film within the trench. Claim 11 includes the additional limitation that the second insulating film comprises a silicon nitride film. Again, no corresponding steps are disclosed or suggested by the prior art of record.

Claims 12-13 depend on claim 10 and include the additional limitation that the thickness of the second insulating film falls within a range of 0.3 to 1.0 μm (claim

12) and that the second insulating film comprises a silicon nitride film (claim 13). No corresponding features of the vertical MOS transistor manufactured according to the method of the present invention are disclosed or suggested by the prior art of record.

Claim 14 includes the additional limitations that the etching back step includes the step of etching back the intermediate insulating film so as to planarize the main surface of the semiconductor substrate, and that the step of forming the source metal electrode comprises the step of forming the source metal electrode as a planar structure. By these steps, the source metal electrode can be formed so as to cover the entire main surface of the semiconductor substrate so that a contact area between the source metal electrode and the source and body contact regions is increased to thereby substantially reduce a resistance therebetween. No corresponding steps are disclosed or suggested by the prior art of record. For example, Ninomiya does not disclose a step of etching back an intermediate insulating film so as to planarize (i.e., flatten) the main surface of the semiconductor substrate.

Furthermore, Ninomiya does not disclose or suggest a source metal electrode having a planar structure formed over a planarized main surface of the semiconductor substrate. In

this regard, a wiring layer 23 (Fig. 8B) in Ninomiya is not planar. Thus, with the method of Ninomiya, it becomes difficult to reduce a resistance between the wiring layer 23 and the source and base regions 17, 16a since a contact hole 20 must be formed therebetween. In order to reduce the resistance, Ninomiya discloses the use of a conductive plug 18 filled in the hole 20 (Fig. 6A; col. 9, lines 18-20).

New claims 15-17 are directed to the formation of the source metal electrode as a planar structure (claims 15-18) so as to cover the entire main surface of the semiconductor substrate (claim 16), and so as to increase a contact area between the source metal electrode and the source and body contact regions to thereby substantially reduce a resistance therebetween (claim 17). Again, no corresponding steps are disclosed or suggested by the prior art of record.

Claim 18 includes the additional step of etching back the intermediate insulating film so as to planarize the main surface of the semiconductor substrate to facilitate formation of the source metal electrode as a planar structure over the main surface of the semiconductor substrate. Again, no corresponding steps are disclosed or suggested by the prior art of record.

In view of the foregoing amendments and discussion, the application is believed to be in allowable form. Accordingly, favorable reconsideration and allowance of the claims are most respectfully requested.

Respectfully submitted,

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